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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/500,580	07/01/2004	Masahiro Sakurada	120222	5256

25944 7590 11/14/2005

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EXAMINER	
LEE, CALVIN	
ART UNIT	**PAPER NUMBER**
2818	

DATE MAILED: 11/14/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/500,580	SAKURADA et al.	
	Examiner	Art Unit	
	Lee, Calvin	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *October 14, 2005 (Election)*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *14-26* is/are pending in the application.

4a) Of the above claim(s) *26* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *14-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *7/01/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

OFFICE ACTION

Response to Election

1. Applicant's argument with respect to the Restriction in the last Office Action is unpersuasive. The Examiner notes that the SOI wafer in Group B may be an FZ wafer, an epitaxial wafer, a nitrogen doped wafer, a hydrogen annealed wafer, an intrinsic gettering wafer, an entire N-region wafer, etc., while the SOI wafer in Group B must be a hydrogen annealed wafer having a step annealing hydrogen ions to form an ion-implanted layer inside a bond wafer.

According to the Response to Restriction received on October 14, 2005, the election of claims 14-25 and the withdrawn of claim 26 are acknowledged.

Double Patenting

2. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b). Effective January 1, 1994, a registered attorney or agent of record may sign the terminal disclaimer.

3. Claims 14-25 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 1 of US Pat. 6,913,646 to *Sakurada et al* in view of US Pat. 2005/0032331 to *Nakano*.

a) Examined claim 14 with its conflicting features is unpatentably rejected over patent claim 1: Si single crystal grown by Czochralski method, occupied by N region outside OSF (in a ring shape) and found no defect region, which is detected by Cu deposition.

Although the patent claim 1 discloses "a silicon single crystal wafer grown by ..." but not "a SOI wafer in which at least a silicon active layer is formed on a support substrate, wherein the silicon active layer consists of silicon single crystal grown by ..." the patent claim 1 inherently anticipates the examined claim 14 because a silicon single crystal wafer is a silicon wafer consisted of a silicon active layer (SOI layer) formed on a support substrate. Nevertheless, that wafer (a SOI wafer) can be called a silicon single crystal wafer, which has been known in the semiconductor processing art as evidenced also by *Nakano* disclosing a formation of the SOI wafer [Fig. 1(h)] having a silicon active layer **7** (also called a SOI layer) formed on a support substrate **2** [Fig. 1(e)].

b) In re claim 15, the patent claim(s) do not suggest, "a thickness of the silicon active layer is 200nm or less." *Nakano* suggests "SOI layer has a thickness of 100nm" [¶ 0067].

It would have been an obvious matter of design choice to have the claimed layer's thickness, since such a modification would have involved a mere change in the size of a SOI wafer and its layers. A change in size is generally recognized as being within the level of ordinary skill in the art. *In re Rose*, 105 USPQ 237 (CCPA 1955).

c) In re claims 16-17, the patent claim(s) do not suggest, "the silicon active layer is formed by being bonded to the support substrate via an oxide film." *Nakano* discloses a silicon active layer **7** being bonded to a support substrate **2** via an oxide film **3** [Fig. 1(g) and ¶ 0057].

It would have been obvious to one having skills in the art to modify the process claim(s) of *Sakurada et al* '646 by utilizing an insulating film sandwiched between a silicon active layer (i.e., a SOI layer) and a support substrate for the purpose of bonding the SOI layer so its surface can be grinded or polished, thereby producing a SOI wafer having a predetermined thickness.

d) In re claims 18-19, the patent claim(s) do not suggest "a thickness of the oxide film is in the range from 2 to 3000nm." *Nakano* discloses "an extremely thin insulator film having a thickness of 0.4μm or less" [¶ 0054].

It would have been an obvious matter of design choice to have the claimed film's thickness, since such a modification would have involved a mere change in the size of a SOI wafer and its films. A change in size is generally recognized as being within the level of ordinary skill in the art. *In re Rose*, 105 USPQ 237 (CCPA 1955).

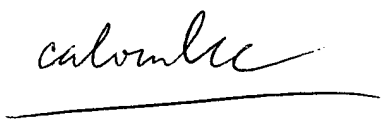
e) In re claims 20-25, the patent claim(s) do not suggest, "the SOI wafer is produced by ion implantation delamination method." *Nakano* discloses a bond wafer **1** being delaminated at a micro bubble layer **4** (also called ion-implanted layer) [¶ 0058-0060].

It would have been obvious to one having skills in the art to modify the process claim(s) of *Sakurada et al* '646 by utilizing ion implantation delamination for the purpose of cleaving/removing a part of the bonded wafer (i.e., a structure comprising the SOI layer 7 and the oxide film **3**) at the ion-implanted layer in order to form a SOI wafer.

Contact Information

4. Any inquiry concerning this communication from the Examiner should be directed to *Calvin Lee* at (571) 272-1896 on Mondays thru Thursdays 6:30-4:30PM. If attempts to reach the examiner by telephone are unsuccessful, Art Unit 2818's Supervisory Patent Examiner *David Nelms* can be reached at (571) 272-1787. The fax phone number for the organization (where this application is assigned to) is (703) 872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system at http:/pair-direct.uspto.gov. Should you have questions on access to the PAIR system, contact the Electronic Business Center at (866) 217-9197.



Calvin Lee

Date: November 10, 2005